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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/762,658	01/22/2004	Dean Z. Tsang	302798.3001-101	5151

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EXAMINER	
PHAM, LONG	
ART UNIT	**PAPER NUMBER**
2814	

DATE MAILED: 10/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/762,658	TSANG, DEAN Z.	
	Examiner	Art Unit	
	Long Pham	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 August 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Rejections and/or objections as previously applied

Claim Rejections - 35 USC § 102

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 1, 6, and 7 are rejected under 35 U.S.C. 102(a) as being anticipated by Misewich et al. (US patent 6,365,913).

With respect to claim 1, Misewich et al. teach a transistor device comprising (see claims 1-40 and associated figures):

a source;

a drain;

a gate;

a metal channel

or channel layer;

With respect to claims 6 and 7, Misewich et al. further teach that the transistor comprises of an enhancement or depletion mode device. See col. 1, lines 57-64.

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 2, 3, 4, and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Misewich et al. (US patent 6,365,913) as applied to claims 1, 6, and 7 above, and further in view of Chu et al. (US publication 2004/0227154).

With respect to claims 4 and 5, Misewich et al. fail to teach the ranges for the thicknesses of the channel layer.

Chu et al. teach a MOS device in which the thickness of channel is between 1 .5 to 2.0 nm . See [00501].

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to use the range for the thickness of channel of Chu et al. in the device of Misewich et al. to achieve enhanced hole mobilities. See (00501.

With respect to claim 3, the use of silicon as substrate material is well-known.

With respect to claim 2, Misewich et al. fail to teach that the channel is located between a gate insulator and an insulator.

However, the formation of a channel over a SOI substrate (including an insulator) and a gate insulator over the channel is well-known.

Claims 8, 9, 10, 11, 12, 13, 14, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wei et al. (US publication 2004/0169227) in combination with Misewich et al. (US patent 6,365,913), Song et al. (US patent 2004/0149579), and Ogura et al. (US publication 2002/0045319).

With respect to claim 8, Wei et al. teach a field effect transistor comprising (see figs. 1 and 2A-2B and associated text):

a channel 33 over an insulator 30B;

a source and a drain 52; and

a gate 36 and a gate insulator 34 over the channel.

Wei et al. fail to teach that the channel is made of metal.

Misewich et al. teach channel made of metal to attain high density memory device, See claims 1-40 and col. 5, lines 60-62.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to use metal as channel material to obtain above advantage,

With respect to claim 9, Wei et al. further teach the insulator further comprises an insulating layer 30B over a substrate 30A, the channel being positioned between the gate and the insulating layer and the gate insulator being positioned under the gate and over the channel.

With respect to claim 10, the use of silicon as substrate material is well-known.

With respect to claim 11, Wei et al. fail to teach the range for the thickness of the channel layer.

Chu et al. teach a MOS device in which the thickness of channel is between 1 .5 to 2.0 nm . See [0050].

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to use the range for the thickness of channel of Chu et al. in the device of Wei et al. to achieve enhanced hole mobilities. See [0050].

With respect to claim 12, Wei et al. further teach the device comprises of a CMOS device. See [0007] .

With respect to claim 13, Wei et al. further teach an encapsulation layer 21. See fig. 1.

With respect to claim 14, Wei et al. fail to teach the range for the width of the channel.

Song et al. teach a channel having width of less than 500 nm. See claim 4.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to use the range for width of the channel of Song et al. in the device of Wei et al. to achieve the benefit of controlling current flow through the channel by controlling the voltage applied across the channel. See [0005].

Further with respect to claim 14, Wei et al. fail to teach the range of the length of the channel.

Ogura et al. teach a channel having a length of 40 nm to reduce voltage and increase speed. See [0024].

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to use the length of the channel of Ogura et al. in the device of Wei et al. to achieve above advantage.

With respect to claim 15, the formation of channel having plurality of layers is well-known.

Response to Arguments

Applicant's arguments filed 08/19/05 have been fully considered but they are not persuasive. See below.

In response to the applicant's arguments in the third paragraph on page 4, the paragraph connecting pages 4 and 5, and the first full paragraph on page 5 of the applicant's response dated 08/19/05, it is submitted that claims 1-40 of Misewich et al. reference teach the use of metal channel layer. Further, it is submitted that the channel layer of Misewich et al. is conductive. Further, it is submitted that a prior art reference is evaluated by what it suggests to one versed in the art, rather than by its specific disclosure. In re Bozek, 163 USPQ 545 (CCPA 1969). Further, it is submitted that a reference is considered not only for what it expressly states, but for what it would reasonably have suggested to one of ordinary skill in the art. In re DeLisle, 160 USPQ (CCPA 1969).

In response to the applicant's arguments in the second full paragraph on page 5 and the paragraph connecting pages 5 and 6, it is submitted that Chu et al. is being relied on only for the teaching of using channel thickness of 1.5 to 2.0 nm to enhance hole nobilities. Further, it is submitted that the use of the above channel thickness would partly contribute to the enhancement of hole nobilities.

In response to the applicant's arguments in the bottom paragraphs on page 6, it is submitted that Wei et al. in combination with Misewich et al., Song et al., and Ogura et al. teach the claimed invention.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is

filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Long Pham whose telephone number is 571-272-1714. The examiner can normally be reached on Mon-Frid, 10am to 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Long Pham
Primary Examiner
Art Unit 2814

LP